

QUESTION 1

- A) The ALU is the Arithmetic and Logic Unit. It performs the arithmetic and Boolean functions between the data in the working register and the file register.

The program counter holds the address of the next instruction.

TRISA is the data register for PORTA and TRISB for PORTB.

- B) Instructions take a certain number of clock cycles to execute. For example, No operation (NOP) takes 4 clock cycles but a RETURN instruction takes 8 clock cycles.

- C) RISC are reduced Instruction Set Computers. It utilises a small, highly optimised set of instructions. It is better for fast operations but unable to handle complex tasks.

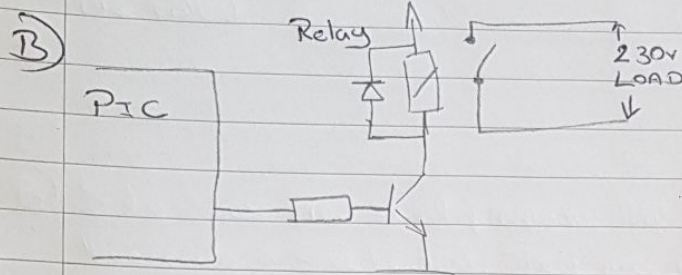
- D) For a time critical process I would use an Assembly Language program, due to variations in Compilers it can be quicker to execute than 'high' level languages.

## QUESTION 2

- A) The stack holds the address of the next counter when subroutines are called.
- B) Subroutines are small programs that are called by the main program to execute a specific task. They are used to break the program down into more manageable bits when writing. As the same subroutine ~~can~~ can be called multiple times it reduces the amount of code needed to be written. Any errors in the subroutine can more easily be rectified.
- C) The PIC16F84 has a unique external interrupt pin RBO. When an interrupt occurs the code that is attached with interrupt is immediately run, once it is finished ~~then~~ it returns to the main code. To ensure correct program operation following the interrupt the last program location needs to be stored so it can be recalled again once the interrupt has finished.

## QUESTION 3

A) The PIC16F84 has a low output DC voltage of 5.5V



PIC can use a relay for a greater AC load. The diode is used to remove the negative voltage produced in the coil.

C) The signal can 'bounce' due to the flexibility of the mechanical switch. A method to ensure safe reliable interfacing would be to read the state of the switch a number of times. Read and record the value and when a switch operation has occurred continue to read the value until a consecutive number of same results has occurred.

D) 12 bits = 4096 levels

$$\text{Value of each level is } \frac{10}{4096} = 2.44 \times 10^{-3}$$

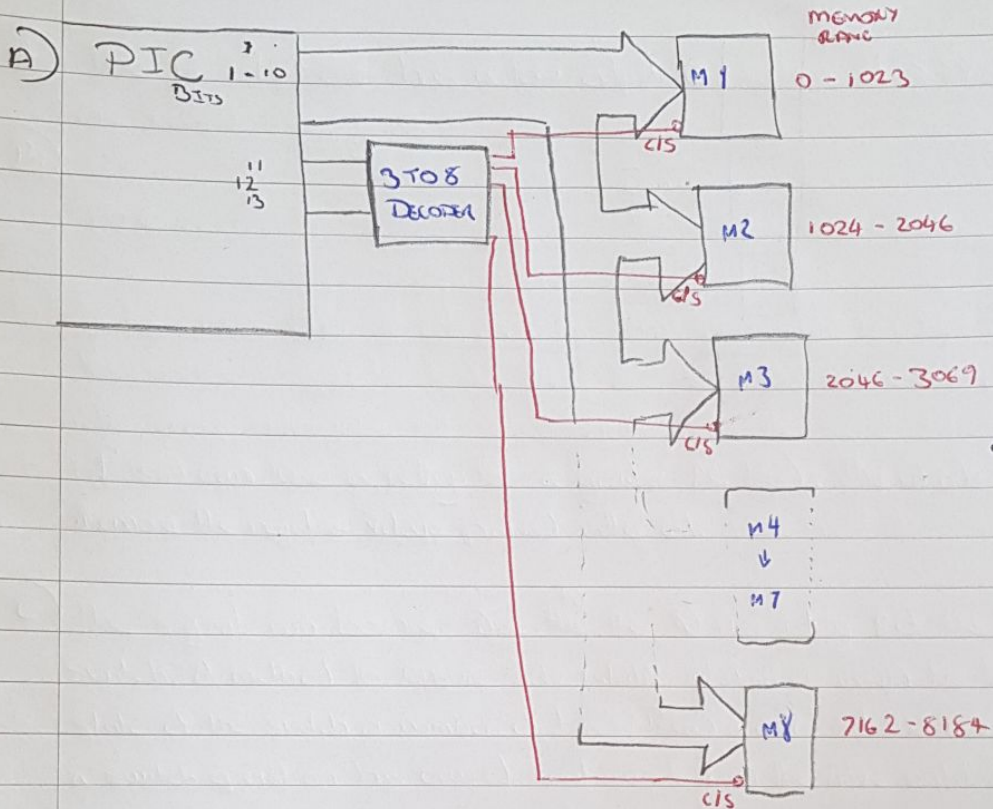
$$\text{Input Voltage } \frac{6.5\text{V}}{2.44 \times 10^{-3}} = 2663.934\text{V round to nearest number} = 2664\text{V}$$

2664 in binary is

|      |      |     |    |    |    |   |   |   |   |
|------|------|-----|----|----|----|---|---|---|---|
| 512  | 256  | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
| 2048 | 1024 |     |    |    |    |   |   |   |   |
| 1    | 0    | 1   | 0  | 0  | 1  | 1 | 0 | 1 | 0 |

Binary Code for 6.5V is 101001101000

QUESTION 4



| 4 | 2 | 1 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---|---|---|-----|-----|-----|----|----|----|---|---|---|---|
| 0 | 0 | 0 | 1   | 1   | 1   | 1  | 1  | 1  | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1   | 1   | 1   | 1  | 1  | 1  | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1   | 1   | 1   | 1  | 1  | 1  | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1   | 1   | 1   | 1  | 1  | 1  | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1   | 1   | 1   | 1  | 1  | 0  | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1   | 1   | 1   | 1  | 0  | 1  | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1   | 1   | 1   | 0  | 1  | 1  | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1   | 1   | 0   | 1  | 1  | 1  | 1 | 1 | 1 | 1 |

## QUESTION 4 CONT.

B) 4699 as a decimal is

4096 2048 1024 512 256 128 64 32 16 8 4 2 1

1 0 0 1 0 0 1 0 1 1 0 1 1

MEMORY CASE 5

LOCATION 603

C) The Von Neumann architecture has the CPU and memory connected with one ~~1~~ data bus which can create a bottle neck. With the data and ~~mem~~ program memory stored in the same chip there is a possibility of overwriting the program area.

The Harvard architecture has separate data and program areas connected by multiple buses which allows the manipulation of data and programs at the same time. With the program area being ROM the program cannot be overwritten.

QUESTION 5

- a) DMA allow Input/Output devices to send and receive data directly from the memory bypassing the CPU. There are three main modes of transfer:
- Burst Mode; the DMA controller gain control over the system bus and only releases after completion of data transfer.
  - Cycle Stealing Mode; the DMA controller forces the CPU to stop its operation and takes control over the system bus for a short term. After the transfer of every byte the DMA releases the bus.
  - Transparent Mode; the DMA only takes control over the system bus if the CPU does not require it.
- b) Synchronous interfaces are synchronised by an external clock. Asynchronous interfaces uses a near constant 'bit' timing.
- c) The  $I^2C$  interface has 2 lines of communication (SDA & SCL) which allows it to easily have multiple slave devices connected to it. The SPI needs 4 lines for each slave limiting the number of slaves due to the increasing complexity of producing a dedicated line for each slave. The SPI, however, can have synchronous data transfer from master to slave. The  $I^2C$  interface can only send 1 data transfer at a time.
- d)  $I^2C$  starts a message transfer by pulling down the SCL and ends the message transfer by pulling the SCL back up.

END